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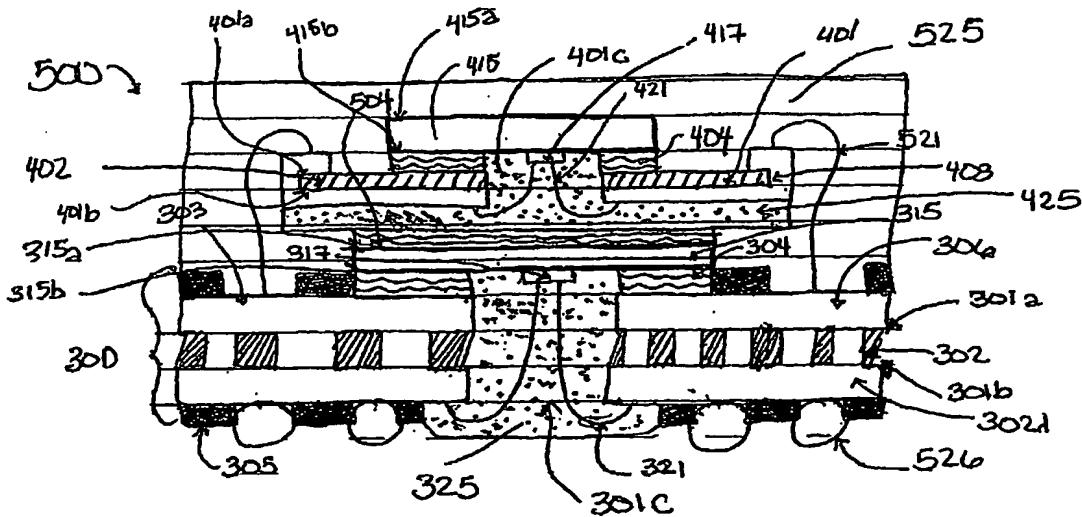
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[Continued on next page]

**(54) Title: MULTI-CHIP BALL GRID GRID ARRAY PACKAGE AND METHOD OF MANUFACTURE**



**(57) Abstract:** A BGA package (500) is disclosed including a base IC structure (300) having a base substrate (302), with an opening (301c) running lengthwise therethrough. A first semiconductor chip (315) is mounted face-down on the base substrate (301) so that the bond pads (317) thereof are accessible through the opening (301c). The package (500) also includes a secondary IC structure (400) including a secondary substrate (401), having an opening (401c) running therethrough, and a second semiconductor chip (415). The second chip (415) is mounted face-down on the secondary substrate (401) so that the bond pads (417) thereof are accessible through the opening (401c) in the secondary substrate (401). An encapsulant (425) fills the opening (401c) in the secondary substrate (401) and forms a substantially planar surface (425a) over the underside of the secondary substrate (401). The substantially planar surface (425a) is mounted to the first chip (315) of the base IC structure (300) through an adhesive (504). Wires (521) connect a conductive portion (406) of the secondary IC structure (400) to a conductive portion (303) of the base IC structure (300).



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- *with amended claims and statement*

**(15) Information about Correction:**

**Previous Correction:**

see PCT Gazette No. 53/2004 of 29 December 2004, Section II

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*For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.*

**AMENDED CLAIMS**

[received by the International Bureau on 03 December 2004  
(03.12.2004);  
original claims 1, 5, 8 and 9 amended; original claims 3 and 4 cancelled ;  
remaining claims unchanged (4 pages)]

**1. A ball grid array package comprising:**

a base IC structure, the base IC structure comprising:

a base substrate having a first base substrate face, a second base substrate face opposite to said first base substrate face, a base substrate opening extending between said first base substrate face and said second base substrate face, and a base conductor;

a first semiconductor chip, comprising a first chip face, a second chip face opposite to said first chip face, and first bond pads disposed over said base opening; and

a first plurality of wires disposed to pass through said substrate base opening and electrically connecting said first bond pads to said base conductor; and

a secondary IC structure, comprising:

a second substrate having a first secondary substrate base, a second secondary substrate face opposite to said first secondary substrate face, a secondary opening extending between said first secondary substrate face and said second secondary substrate face, and a secondary conductor;

a second semiconductor chip, comprising a second chip face, and a second bond pad disposed over said secondary opening; and

a second plurality of wires electrically connecting said second bond pads to said secondary conductor through said secondary opening; and

a first encapsulant filling said secondary opening around said second plurality of wires and covering said second secondary substrate face; and

said secondary IC structure being mounted on said base IC structure, and further comprising a third plurality of wires connecting said secondary IC structure to said base IC structure.

2. A ball grid array package according to claim 1, wherein:

    said base substrate further comprises a plurality of vias extending between said first base substrate face and said second base substrate face;

    said base conductor extends through said vias; and

    said base substrate further comprises a layer of solder mask disposed on portions of said first and second chip faces.

3. Cancelled.

4. Cancelled.
5. The ball grid array package according to claim 1, further comprising molding compound encapsulating at least portions of said base IC structure and said secondary IC structure.
6. The ball grid array package according to claim 5, wherein said molding compound encapsulates said third plurality of wires.
7. The ball grid array package according to claim 5, wherein said first secondary chip face is free of said molding compound.
8. The ball grid array package according to claim 1, further comprising:

at least one additional of said secondary IC structure mounted over said first secondary chip face; and

respective wires connecting a conductive portion of said at least one additional secondary IC structure to said base IC structure.

9. The ball grid array package according to claim 1, further comprising a thermal dissipation element disposed over said first secondary chip face.

10. A method of assembling a ball grid array package, comprising:

providing a base IC structure, comprising a base substrate and a first semiconductor chip mounted on said base substrate in a die-down configuration;

linking the bond pads of the base chip to the base substrate using the first plurality of wires;

providing a first secondary IC structure, comprising a secondary substrate and a second semiconductor chip mounted on said second substrate in a die-down configuration;

mounting the first secondary IC structure to said base IC structure;

electrically connecting a conductive portion of said secondary IC structure to a conductive portion of said base IC structure using at least a second plurality of wires, and

encapsulating said base IC structure and said first secondary IC structure, including said first plurality of wires and said second plurality of wires.

11. The method of claim 10, wherein said encapsulating step comprises first encapsulating said first secondary IC structure and subsequently encapsulating said base IC structure and said first secondary IC structure, together with said first and second plurality of wires.

**STATEMENT UNDER ARTICLE 19(1)**

The claims have been amended to describe the invention more particularly, and do not narrow the scope of the claims. No new matter has been added.